Application of AI to Accelerate Formal Verification Workflow

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Abstract:

Formal verification is essential for ensuring correctness in safety-critical hardware systems. However, setting up formal verification tasks remains labor-intensive, requiring manual configuration of the environment and RTL module integration via Tcl scripts, and binding interfaces to SystemVerilog assertions. The process becomes increasingly cumbersome with large signal sets or when reusing across projects.

This paper investigates the application of AI-assisted tools, specifically GitHub Copilot, to automate and streamline key aspects of the formal verification workflow. Our approach automates the generation of interface scripts by extracting RTL input/output pins and adapting them to diverse projects. It also facilitates the migration of existing formal verification tasks with minimal manual intervention. A novel contribution is the use of AI to generate SystemVerilog properties directly from Finite-State Machine (FSM) diagrams in design specifications. These properties are successfully verified using Synopsys VC Formal. Applied across multiple projects in Formal Property Verification (FPV) and Formal Register Verification (FRV), the method also extends to Sequential Equivalence Checking (SEQ), Connectivity Checking (CC), and Data Path Verification (DPV).

Results show significant reductions (more than 1.5x) in setup time and manual effort. Overall, this paper demonstrates AI's potential to enhance automation in general applications of formal methods.