CDC Techniques Without Synchronizers: Holistic Approach for High Quality Low Power Design

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ABSTRACT:

Achieving a high-quality low power design requires robust “clock domain crossing (CDC)” analysis. In traditional CDC methodologies, the use of multi-flop synchronizers is standard for safe signal transmission across asynchronous clock domains. However, in low power designs, this approach introduces additional logic that negatively impacts power, performance, and area (PPA) - key metrics for SoC efficiency.

This paper explores design techniques that address CDC violations by minimizing logic addition, defining architectural timing requirements and the using delay buffers, provided with a bound maximum delay from the synthesis team, to ensure safe signal transfer. Comparative analysis demonstrates that this approach not only satisfies CDC correctness but also supports waiver-free signoff, enabling high-confidence delivery without compromising PPA.