

Machine-Learning-Assisted Floorplan-Aware NoC Topology Synthesis Framework for Complex SoCs

PRESENTER: Siying Liu / Senior MTS Silicon Design Engineer / **AMD**

ABSTRACT:

This paper presents a novel NoC topology design approach that integrates numerous IPs under complex physical and power domain constraints based on floorplan. By leveraging ML clustering and MST algorithms, we achieve optimal area and latency, reducing 90% effort and 5% area.