ABSTRACT

Optimizing ECO Efficiency and Precision: an alternative approach for Implementing Digital-Intensive RTL Module Restructuring Through Metal Changes in IC Design

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In integrated circuit (IC) design, an Engineering Change Order (ECO) enables late-stage device modifications without a full chip redesign, offering a cost-effective and time-efficient solution for addressing design errors, performance issues, or specification changes. Metal ECOs are preferred over a full mask ECO, whenever feasible, due to their flexibility and reduced impact on cost and schedule. However, most of the time it is the entity of the changes to determine the metal fix feasibility. While minor changes usually require manual updates to the post-layout netlist, with minimal impact on timing and design rule checks (DRC), bigger changes raise concerns about spare cells availability and DRC feasibility. To manage this, a specialized tool is employed, but the process is iterative and complicated by the tool's lack of clock-tree awareness, causing timing and clock balancing issues. Challenges also include insufficient or distant spare cells causing design rule violations, and the tool's inability to utilize unused cone logic, limiting the reuse of existing cells. In this study, we present the alternative methodology employed for the comprehensive redesign of a whole digital RTL module within a digital top-level circuit, highlighting the challenges encountered and the strategies adopted to facilitate the metal ECO fix over a full mask ECO, therefore bringing a significant cost-reduction in the manufacturing process.