Low-Power Architectures for Clock Domain Crossing in SoC Design

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ABSTRACT:

This paper proposes innovative low-power architectures to tackle clock domain crossing (CDC) challenges in modern SoC designs. It introduces high figure-of-merit solutions for both data and control path interfacing, ensuring robust performance and energy efficiency. The approach significantly reduces the number of required registers in the data path by leveraging optimal clock phase selection, while also improving latency. For control signal synchronization, a novel mechanism is introduced that minimizes flip-flop usage and ensures clock gating in the destination domain.

This design activates the destination clock only upon input changes, further enhancing power efficiency. Additionally, the paper outlines a method to eliminate traditional reset synchronizers by intelligently delaying reset de-assertion. The proposed techniques are validated through detailed timing analysis and chronograms.