Application of AI to Accelerate Formal verification workflow

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Abstract

Formal verification is critical for ensuring correctness in safety-critical hardware systems. However, the setup process remains labor-intensive, requiring configuration of the environment manually, RTL integration via Tcl scripts, and binding interfaces to SystemVerilog (SV) assertions. These tasks become increasingly complex with large signal sets or when properties requiring being reused across various configurations. This paper presents a methodology to automate key aspects of the formal verification workflow with AI-assistant. The approach includes Python script generation for RTL interface extraction, environment setup, and regression integration. The major contribution of the work presented in this paper is automatically implementing SystemVerilog properties based on prompts fed in AI tool. These properties are successfully verified using Synopsys VC Formal (VCF) after being reviewed by verification Engineers. With AI-assistance, the formal verification tests can also be launched in regression efficiently and the regression results are automatically sent to test owners. Applying this method, time consumed in formal verification flow has been largely reduced. Although the experiments are conducted using VCF, the methodology is tool-agnostic and applicable to other formal platforms such as JasperGold and Questa Formal.