The Motivation and Needs

The goal of this project is to implement the computation of frame synchronization (frame sync) in an FPGA to reduce the processing burden on the CPU of an SDR (Software Defined Radio) platform, and to exploit the parallelism inherent in a hardware implementation.

Theory (Preamble Explanation)

In order to identify the message that is hidden inside the spectrum there must be a known signal that can be searched for. This signal is agreed upon by both the transmitter and the receiver. In this implementation the preamble used is shown below. It is generated by taking a known sequence of 32 1’s and -1’s and then passing them through a Square Root Raised Cosine Filter. This filter is used by the matched filter for the filtering.

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